or higher than the impurity concentration of said epitaxial layer, wherein the depth of said second embedded diffusion layer is deeper than that of said first embedded diffusion layer, and wherein a peak position of an impurity concentration of a region formed between said silicon substrate and a base region of said second vertical type bipolar transistor is deeper than that of a region formed between said silicon substrate and a base region of said first vertical bipolar transistor.

17. (Amended) A semiconductor device according to claim 1, further comprising:
a third vertical type [PNP] bipolar transistor having a separating diffusion layer formed in an upper part of said silicon substrate for separating from said silicon substrate a third embedded diffusion layer having an opposite conductive type to that of said epitaxial layer.

REMARKS

Claims 1, 3, 4, 6, 17, 19 and 20 are pending in the application. In the Office Action of July 25, 2000, the Examiner made the following objections and rejections:

A.) Objected to the drawings.

B.) Objected to claim 17 for an informality.

C.) Rejected claims 1, 3, 4, 6, 19 and 20 under 35 U.S.C. §103(a) as being unpatentable over *Kumamaru et al.* or *Watanabe et al.*

D.) Rejected claim 17 under 35 U.S.C. §103(a) as being unpatentable over *Kumamaru et al.* or *Watanabe et al.* in view of *Takemoto et al.*

Applicants respectfully traverse the rejections and addresses the Examiner's objections and rejections as follows:

A.) Objection to the drawings:

The Examiner stated that the drawings do not show a device comprising first, second and third transistors, being formed on one substrate, as recited in claim 17. Applicants respectfully disagree.

FIG. 5 shows a first transistor 101 and a second transistor 102 formed on a substrate 110. FIGs. 11 and 12J show that a third transistor 103 can also be formed on the same substrate 110 as the first and second transistors 101, 102. (See, also, Specification page 59, lines 17-22).

Applicants respectfully submit that the objection has been overcome and request that it be withdrawn.

B.) Objection to claim 17 for an informality:

Claim 17 has been amended as per the Examiner's request to overcome the objection.

Applicants respectfully submit that the objection has been overcome and request that it be withdrawn.

C.) Rejection of claims 1, 3, 4, 6, 19 and 20 under 35 U.S.C. §103(a) as being unpatentable over *Kumamaru et al.* or *Watanabe et al.*:

Applicants respectfully disagree with the Examiner's rejection.

Applicants' present invention claims a semiconductor device having a first vertical type bipolar transistor and a second vertical type bipolar transistor. The first and second bipolar transistors are formed on a substrate by forming an epitaxial layer on a silicon substrate. The first vertical type bipolar transistor has a first embedded diffusion layer formed in an upper part of the silicon substrate. The first embedded diffusion layer has an impurity concentration higher than that of the epitaxial layer. The second vertical bipolar transistor has a second embedded diffusion layer formed in an upper part of the silicon substrate. The second embedded diffusion layer has an impurity concentration which is less than the impurity concentration of the first embedded diffusion layer and is approximately equal to or higher than the impurity concentration of the epitaxial layer. The second embedded diffusion layer has a depth which is greater than a depth of the first embedded diffusion layer. A peak position of an impurity concentration of a region formed between the silicon substrate and a base region of the second vertical type bipolar transistor is deeper than that of a region formed between the silicon substrate and a base region of the first vertical bipolar transistor.

This is unlike either *Kumamaru et al.* or *Watanabe et al.*, both of which fails to disclose or suggest a second embedded diffusion layer having an impurity concentration which is less than the impurity concentration of a first embedded diffusion layer. In fact, *Kumamaru et al.* discloses a second embedded diffusion layer 12 and a first embedded diffusion layer 14 which have an equal impurity concentration of $1x10^{19}/cm^3$ to $5x10^{19}/cm^3$. (Col. 4, lines 9-13). Therefore, *Kumamaru et al.* fails to disclose or suggest Applicants' second embedded diffusion layer. Further, the Examiner mistakenly refers to the *Kumamaru et al.* $n^-$-type epitaxial layer 5a as an embedded diffusion layer. However, this layer 5a is not an equivalent structure to Applicants' second embedded diffusion layer.

Further, neither *Kumamaru et al.* nor *Watanabe et al.*, taken singly or in combination, disclose or suggest a peak position of an impurity concentration of a region formed between a

silicon substrate and a base region of the second vertical type bipolar transistor which is deeper than that of a region formed between the silicon substrate and a base region of the first vertical bipolar transistor. In fact, *Watanabe et al.* discloses a peak position of an impurity concentration of a region formed between a silicon substrate and a base region of an NPN transistor 101 which is equal to that of a region formed between the silicon substrate and a base region of an $I^2L$ 201.

Therefore, neither *Kumamaru et al.* nor *Watanabe et al.*, taken singly or in combination, disclose or suggest Applicants' present invention.

Applicants respectfully submit that the rejection of claims 1, 3, 4, 6, 19 and 20 has been overcome and request that it be withdrawn.

D.) Rejection of claim 17 under 35 U.S.C. §103(a) as being unpatentable over *Kumamaru et al.* or *Watanabe et al.* in view of *Takemoto et al.*:

Applicants respectfully disagree with the Examiner's rejection.

Applicants' claim 1 is allowable over *Kumamaru et al.* and *Watanabe et al.* as discussed above. *Takemoto et al.* still fails to disclose or suggest Applicants' claimed second embedded diffusion layer or peak position of an impurity concentration.

Therefore, none of *Kumamaru et al.*, *Watanabe et al.*, nor *Takemoto et al.*, taken singly or in combination, disclose or suggest Applicants' claim 1.

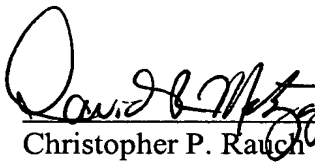
Claim 17 depends directly or indirectly from claim 1 and is therefore allowable for at least the same reasons that claim 1 is allowable.

Applicants respectfully submit that the rejection of claim 17 has been overcome and request that it be withdrawn.

## CONCLUSION

In view of the foregoing, it is submitted that claims 1, 3, 4, 6, 17, 19 and 20 are patentable. It is therefore submitted that the application is in condition for allowance. Notice to that effect is respectfully requested.

Respectfully submitted,



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